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(54) Short channel field effect transistor

(57) A low power transistor (10, 30, 50, 50', 70, 70') formed in a face of a semiconductor layer (22, 42, 62, 86) of a first conductivity type. The transistor includes a source and drain regions (16, 18, 36, 38, 56, 58, 76, 78) of a second conductivity type formed in the face of the semiconductor layer, and a gate (12, 32, 52, 72) insulatively disposed adjacent the face of the semiconductor layer and between the source and drain regions. A super-steep retrograde channel (22, 42, 62) of the first conductivity type formed in the semiconductor layer a predetermined distance from the face of the semiconductor layer. A layer of counter doping (44, 66, 66', 80, 80') of the second conductivity type is formed adjacent to the face of the semiconductor layer generally between the source and drain regions. A first and second pockets (82, 84, 82', 84') of the first conductivity type may also be formed generally adjacent to the source and drain regions and the counter doped layer (80, 80').

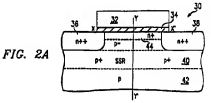

FIG. 2A

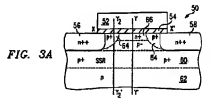

FIG. 3A

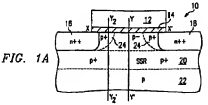

FIG. 1A

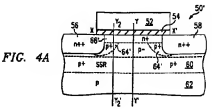

FIG. 4A

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Description

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of semiconductor devices. More particularly, the invention is related to semiconductor devices with super-steep retrograde and/or pocket implant and/or counter doping.

BACKGROUND OF THE INVENTION

Portable personal electronic devices such as cellular telephones, notebook computers, and other peripheral equipment have become increasingly popular for consumers. The current technological challenge in building portable battery-operated equipment is to drastically reduce the power consumption and thus prolong battery life, and still maintain reasonable speed performance. The low standby power demands of CMOS makes it especially suited for this application. Although reducing the power supply voltage, V_{DD}, to 1V or below is very effective in reducing power consumption, it also lowers the speed performance. To lower the supply voltage and still maintain operational speed, the threshold voltage of the transistor, V_T, must also be lowered. The threshold voltage can be reduced by using a lower substrate impurity concentration. However, this increases the undesirable short channel effect in submicron devices. Therefore, it may be seen that the design of a submicron transistor for low power supply voltage operations is non-trivial.

SUMMARY OF THE INVENTION

Accordingly, there is a need for a low power submicron transistor structure that provides low V_T, reduced short channel effect, and good speed performance.

In accordance with the present invention, a low threshold voltage transistor with improved performance is provided which eliminates or substantially reduces the disadvantages associated with prior transistor devices.

In one aspect of the invention, a transistor is formed in a face of a semiconductor. The transistor includes source and drain regions formed in the face of the semiconductor layer with a gate insulatively disposed adjacent the face of the semiconductor layer and between the source and drain regions. A layer of counter doping is introduced in and near the face of the semiconductor layer generally between the source and drain regions. Two pocket implants may also be formed generally adjacent to the source and/or drain regions and the counter doped layer.

In another aspect of the invention, a method of manufacturing a transistor is provided. The transistor is formed in a face of a semiconductor layer having a first conductivity type. The method includes the steps of selectively implanting a shallow layer of impurities of a second conductivity type adjacent to the face of the semiconductor layer and forming pockets of impurities of the first conductivity type generally adjacent to the source and drain regions below the gate. The pockets may also be formed closer to the face of the semiconductor layer with the layer of counter doping therebetween.

In yet another aspect of the invention, a transistor structure includes a surface counter doping layer of the second impurity type formed generally between the drain and source regions, and pocket implants of the first impurity type formed generally adjacent and/or below the counter doping layer.

In another aspect of the invention, a transistor is formed in a face of a semiconductor. The transistor includes source and drain regions formed in the face of the semiconductor layer with a gate insulatively disposed adjacent the face of the semiconductor layer and between the source and drain regions. A super-steep retrograde channel doping profile is disposed in the semiconductor layer a predetermined distance from the face of the semiconductor layer, and a layer of counter doping is introduced in and near the face of the semiconductor layer generally between the source and drain regions. Alternatively or in combination therewith, two pocket implants may also be formed generally adjacent to the source and/or drain regions and the counter doped layer.

In another aspect of the invention, a method of manufacturing a transistor is provided. The transistor is formed in a face of a semiconductor layer having a first conductivity type. The method includes the steps of implanting impurities of the first conductivity type to form a super-steep retrograde channel profile at a predetermined distance below the face of the semiconductor layer, and selectively implanting a shallow layer of impurities of a second conductivity type adjacent to the face of the semiconductor layer. Alternatively or in combination therewith, pockets of impurities of the first conductivity type are implanted generally adjacent to the source and drain regions below the gate.

Technical advantages of the instant invention include a submission transistor structure that has low threshold voltage satisfying the need for high performance at lower power supply voltages for portable electronic equipment. The instant transistor structure(s) satisfies this need with a reduced short channel effect which in turn minimizes the sensitivity of transistor performance to gate length variation at shorter channel lengths.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference should now be made to the accompanying drawings, in which:

FIGURE 1A is a cross-sectional view of a transistor structure in accordance with the present invention with super-steep retrograde channel and pocket

implant;

FIGURE 1B is an exemplary plot of doping concentration versus depth of the transistor structure along Y-Y' as shown in FIGURE 1A;

FIGURE 1C is an exemplary plot of doping concentration versus depth along Y_2-Y_2' in the transistor structure shown in FIGURE 1A;

FIGURE 1D is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 1A;

FIGURE 2A is a cross-sectional view of a transistor structure of the present invention with super-steep retrograde channel and counter doping;

FIGURE 2B is an exemplary plot of doping concentration versus depth of a transistor structure with super-steep retrograde channel and counter doping along Y-Y' as shown in FIGURE 2A;

FIGURE 2C is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 2A;

FIGURE 3A is a cross-sectional view of a transistor structure of the present invention with super-steep retrograde channel, pocket implant, and counter doping;

FIGURE 3B is an exemplary plot of doping concentration versus depth of the transistor structure along Y-Y' as shown in FIGURE 3A;

FIGURE 3C is an exemplary plot of doping concentration versus depth along Y_2-Y_2' in the transistor structure shown in FIGURE 3A;

FIGURE 3D is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 3A;

FIGURE 4A is a cross-sectional view of another transistor structure of the present invention with super-steep retrograde channel, pocket implant, and counter doping;

FIGURE 4B is an exemplary plot of doping concentration versus depth of the transistor structure along Y-Y' as shown in FIGURE 4A;

FIGURE 4C is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 4A;

FIGURE 4D is an exemplary plot of doping concentration versus depth along Y_2-Y_2' of the transistor structure shown in FIGURE 4A;

FIGURE 5A is a cross-sectional view of a transistor structure of the present invention with pocket implant and counter doping;

FIGURE 5B is an exemplary plot of doping concentration versus depth of a transistor structure along Y-Y' as shown in FIGURE 5A;

FIGURE 5C is an exemplary plot of doping concentration versus depth along Y_2-Y_2' of the transistor structure shown in FIGURE 5A;

FIGURE 5D is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 5A;

FIGURE 6A is a cross-sectional view of another transistor structure of the present invention with pocket implant and counter doping;

FIGURE 6B is an exemplary plot of doping concentration versus depth of a transistor structure along Y-Y' as shown in FIGURE 6A;

FIGURE 6C is an exemplary plot of doping concentration versus depth along Y_2-Y_2' of the transistor structure shown in FIGURE 6A; and

FIGURE 6D is an exemplary plot of doping concentration along the surface X-X' of the transistor structure shown in FIGURE 6A.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment(s) of the present invention is (are) illustrated in FIGURES 1-6, like reference numerals being used to refer to like and corresponding parts of the various drawings.

In FIGURE 1A, an nMOS transistor structure 10 includes a gate electrode 12, gate dielectric 14, and source and drain n^{++} regions 16 and 18. A p^+ super-steep retrograde (SSR) channel 20 is further formed at a predetermined distance or depth from the top surface of the device in a p-type substrate or well structure 22. For example, 190 Kev indium (In) at a dose of 1×10^{13} cm^{-2} may be implanted in an nMOS region to form the super-steep retrograde channel 20. In a pMOS device with p^{++} source and drain regions (not shown), the n^+ super-steep retrograde channel 20 may be formed by implanting arsenic (As). When compared with conventional channel doping profiles using boron (B) for nMOS and Phosphorus (P) for pMOS, for example, super-steep retrograde channel profile has been shown to provide better short channel integrity. Further, super-steep retrograde channel doping also provides a higher channel mobility due to lower surface doping.

In addition to the super-steep retrograde channel

profile 20, shallow pocket implants or halos 24 of an opposite type to the source and drain regions 16 and 18 are formed. The pocket implants 24 are generally adjacent and/or below the source and drain regions 16 and 18. For an nMOS device, boron may be used as a typical dopant species for the pocket implant; for a pMOS device, phosphorous may be used to form the pocket implant. Exemplary implant doses of 5×10^{12} to 2×10^{13} cm^{-2} may be used to form the pocket implants. FIGURE 1B is an exemplary plot of doping concentration versus depth for transistor structure 10 along Y-Y', and FIGURE 1C is an exemplary plot of doping concentration along Y_2-Y_2'. In addition, FIGURE 1D is an exemplary plot of surface doping concentration along X-X'.

Transistor structure 10 with both super-steep retrograde channel doping 20 and pocket implants 24 has reduced short-channel effect when compared to a super-steep retrograde only channel profile, described in technical articles such as "Indium Channel Implant for Improved Short-Channel Behavior of Submicrometer NMOSFET's" by Shahidi et al. in *IEEE Electron Device Letters*, Vol. 14, No. 8, p. 409, August 1993; and "Trade-offs of Current Drive vs. Short-Channel Effect in Deep-Submicrometer Bulk and SOI MOSFETs" by Su et al. in *IEEE IEDM*, p. 649, 1994. The pocket implantation process is discussed in "Design/Process Dependence of 0.25 μm Gate Length CMOS for Improved Performance and Reliability" by Rodder et al. in *IEEE IEDM*, p. 71, 1994. Transistor structure 10 also has better short channel integrity when compared to a conventional device with pocket implants described in Rodder et al.

Referring to FIGURE 2A, a transistor structure 30 with super-steep retrograde channel profile and shallow surface counter doping is shown. Transistor structure 30 is shown as an nMOS with a gate electrode 32, gate dielectric 34, and source and drain n^{++} regions 36 and 38. A p-type super-steep retrograde buried channel 40 is formed at a predetermined depth in a p-type substrate or well formation 42. A narrow layer 44 of surface counter doping of n-type (n^*) is formed in the region between source and drain regions 36 and 38 and below gate 32. The counter doping may be formed with, for example, arsenic (As) at a dosage of $2 \text{ to } 4 \times 10^{12}$ cm^{-2} for nMOS or BF_2 for pMOS (not shown). FIGURE 2B is an exemplary plot of doping concentration versus depth of transistor structure 30 taken along Y-Y', and FIGURE 2C is an exemplary plot of surface doping concentration along X-X'. Counter doping is discussed in articles such as "High Performance Sub-0.1-μm CMOS with Low-Resistance T-shaped Gates Fabricated by Selective CVD-W" by Hisamoto et al. in *Symposium on VLSI Technology Digest of Technical Papers*, 1995; and "A Device Design Study of 0.25 μm Gate Length CMOS for IV Low Power Applications" by Nandakumar et al. submitted for publication in the *IEEE Symposium on Low Power Electronics*, October 1995.

Transistor structure 30 combining super-steep retrograde channel 40 and surface counter doping 44 lowers the threshold voltage and maintains good short channel effect. The counter doping 44 provides threshold voltage scaling to the desired range of approximately 0.05 to 0.15 volts, while the underlying super-steep retrograde channel profile 40 is more effective at reducing threshold voltage roll-off than conventional well and channel profile described in Hisamoto et al. Transistor structure 30 also maintains high nominal drive current due to its low threshold voltage and high effective electron mobility μ_{eff}. Therefore, the combination of these features provides optimal performance for low supply voltage CMOS applications.

Referring to FIGURE 3A, a transistor structure 50 with a super-steep retrograde channel profile, pocket implantation, and counter doping is shown. Transistor structure 50 is shown as an nMOS and includes a gate electrode 52, gate dielectric 54, and source and drain regions 56 and 58. A super-steep retrograde channel 60 is implanted subsurface generally below source and drain regions 56 and 58 in a substrate or well structure 62. Pockets 64 are implanted at a shallow depth near the surface and adjacent to source and drain regions 56 and 58. Surface counter doping 66 is also formed generally between implanted pockets 64. An exemplary doping concentration versus depth plot for transistor 50 along Y-Y' is shown in FIGURE 3B, and another exemplary plot of doping concentration along Y_2-Y_2' is shown in FIGURE 3C. A surface doping concentration plot along X-X' of transistor structure 50 is shown in FIGURE 3D.

FIGURE 4A shows one possible variation of the placement of pocket implants with respect to counter doping. Transistor 50' includes pocket implants 64' that are slightly subsurface below the counter doped layer 66'. An exemplary doping concentration versus depth plot along Y-Y' for transistor 50' is shown in FIGURE 4B, surface doping concentration along X-X' is shown in FIGURE 4C, and doping concentration along Y_2-Y_2' is shown in FIGURE 4D.

Transistor structures 50 and 50' combine the advantages of super-steep retrograde channel, pocket implants, and surface counter doping and are both well-suited to low power applications due to their low threshold voltage, reduced short channel effect, and good drive current.

FIGURE 5A is a cross-sectional view of a transistor structure 70 that does not incorporate a super-steep retrograde channel profile and yet still has low threshold voltage and improved short channel effect. Transistor structure 70 includes a gate electrode 72, gate dielectric 74, and source and drain n^{++} regions 76 and 78. Transistor structure 70 further includes a surface counter doping n^* layer 80 in combination with pocket implants 82 and 84 of an opposite type (p^+). As discussed above, the placement of surface counter doping layer 80 and pocket implants 82 and 84 may have a number of variations, all of which are contemplated herein. Exemplary doping concentration in transistor 70 along lines Y-Y' and Y_2-Y_2' are shown in FIGURES 5B and 5C, respectively. An exemplary surface doping concentration of

transistor structure 70 along X-X' is shown in FIGURE 5D.

FIGURE 6A is a cross-sectional view of yet another transistor structure 70' with counter doping and pocket implants. Transistor structure 70' includes a gate electrode 72, gate dielectric 74, and source and drain n^{++} regions 76 and 78. Transistor structure 70' further includes a surface counter doping n^+ layer 80' in combination with pocket implants 82' and 84' of an opposite type (p^+). As discussed above, the placement of surface counter doping layer 80' and pocket implants 82' and 84' may have a number of variations, all of which are contemplated herein. The pocket implants 82 and 84 of FIGURE 5A are formed generally below the counter doping layer 80, but the pocket implants 82' and 84' are formed near the surface. Exemplary doping concentration in transistor 70' along lines Y-Y' and Y_2-Y_2' are shown in FIGURES 6B and 6C, respectively. An exemplary surface doping concentration of transistor structure 70 along X-X' is shown in FIGURE 6D.

Transistors 10, 30, 50, 50', 70, and 70' may be constructed by conventional semiconductor processing technology and may include forming the super-steep retrograde channel, the gate, and drain and source regions. The counted doping may be formed before the formation of the gate. Pocket implant may be formed after gate formation.

The transistor structures, as constructed according to the teachings of the invention, are applicable to both nMOS and pMOS in CMOS technology. Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from the spirit and scope of the invention. More specifically, it is important to note that the chemical compositions, concentrations and other detailed specifications enumerated above serve as illustrative examples and may be substituted by other such specifications as known in the art of semiconductor processing.

Claims

1. A transistor formed in a layer of semiconductor material comprising;

   first and second current guiding regions formed in said semiconductor layer, said first current guiding region being separated from said second current guiding region by a predetermined distance;
   a control region insulatively disposed adjacent a face of said semiconductor layer and substantially between said first and second current guiding regions;
   a counter doping layer formed substantially in and adjacent to said face of said semiconductor layer generally in a region between said first and second current guiding regions; and
   a first pocket and a second pocket formed generally in a region below said control region and adjacent said first and second current guiding regions respectively.

2. A transistor formed in a layer of semiconductor material comprising;

   first and second current guiding regions formed in said semiconductor layer, said first current guiding region being separated from said second current guiding region by a predetermined distance;
   a control region insulatively disposed adjacent a face of said semiconductor layer and substantially between said first and second current guiding regions;
   a channel region formed in said semiconductor layer at a predetermined distance from said face of said semiconductor layer; and
   a counter doping layer formed substantially in and adjacent to said face of said semiconductor layer generally in a region between said first and second current guiding regions.

3. A transistor formed in a layer of semiconductor material comprising;

   first and second current guiding regions formed in said semiconductor layer, said first current guiding region being separated from said second current guiding region by a predetermined distance;
   a control region insulatively disposed adjacent a face of said semiconductor layer and substantially between said first and second current guiding regions;
   a channel region formed in said semiconductor layer at a predetermined distance from said face of said semiconductor layer; and
   a first pocket and a second pocket formed generally in a region below said control region and adjacent said first and second current guiding regions respectively.

4. The transistor as claimed in Claim 2 further comprising;

   a first pocket and a second pocket formed generally in a region below said control region and adjacent said first and second current guiding regions respectively.

5. The transistor as claimed in Claim 1, Claim 3 or Claim 4, wherein said first and second pockets are formed below said first and second current guiding regions.

6. The transistor as claimed in Claim 3 further com-

prising;

a counter doping layer formed substantially adjacent to said face of said semiconductor layer in a region substantially between said first and second current guiding regions.

7. The transistor as claimed in any preceding claim, wherein said semiconductor layer, and said first and second pockets are formed from semiconductor material of a first conductivity type, and said counter doping layer, and said first and second current guiding regions are formed from semiconductor material of a second conductivity type.

8. The tansistor as claimed in any of Claims 2 to 7, wherein said channel region is a super-steepp retrograde channel.

9. A method of manufacturing a low power transistor formed in a semiconductor layer having a first conductivity type, comprising the steps of:

selectively implanting a shallow layer of impurities of a second conductivity type substantially adjacent to said face of said semiconductor layer;
forming a control region insulatively adjacent to said face of said semiconductor layer and substantially above said shallow impurity layer;
forming pockets of impurities of said first conductivity type generally adjacent to said shallow layer of impurities substantially below said control region; and
forming first and second current guiding regions of said second conductivity type disposed substantially on either side of said control region.

10. A method of manufacturing a low power transistor formed a semiconductor layer having a first conductivity type, comprising the steps of:

implanting impurities of said first conductivity type to form a channel region a predetermined distance below said face of said semiconductor layer;
selectively implanting a shallow layer of impurities of a second conductivity type substantially adjacent to said face of said semiconductor layer;
forming a gate insulatively adjacent to said face of said semiconductor layer and substantially above said shallow impurity layer; and
forming a source and drain regions of said second conductivity type disposed substantially on either side of said gate.

11. The method, as set claimed in Claim 10, further comprising the step of forming pockets of impurities of said first conductivity type generally adjacent to said source and drain regions below said gate.

12. The method, as claimed in Claim 9 or Claim 11, wherein the step of forming pockets of impurities of said first conductivity type forms said pockets generally adjacent to and below said source and drain regions.

13. The method, as claimed in Claims 9 to 12, wherein the step of forming pockets of impurities of said first conductivity type comprises forming said pockets generally in and adjacent to said face of said semiconductor layer with said shallow impurity layer therebetween.

FIG. 1A

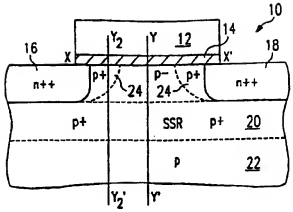


FIG. 1B

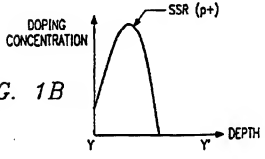


FIG. 1C

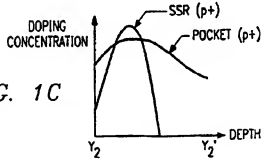
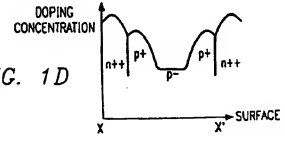


FIG. 1D



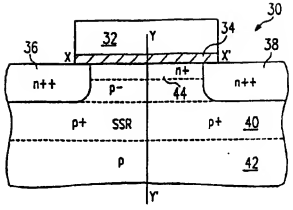


FIG. 2A

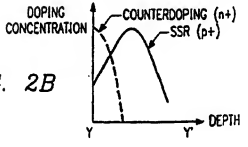


FIG. 2B

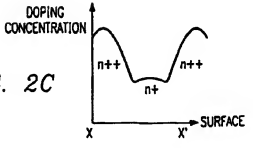


FIG. 2C

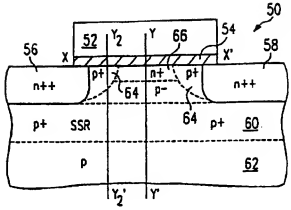


FIG. 3A

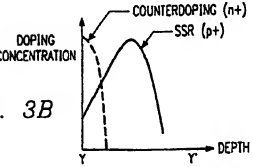


FIG. 3B

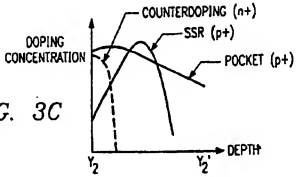


FIG. 3C

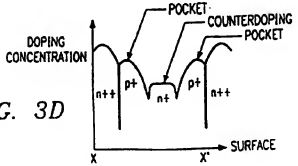


FIG. 3D

FIG. 4A

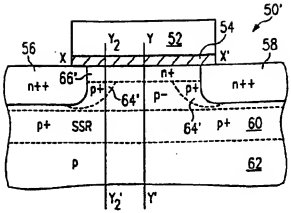


FIG. 4B

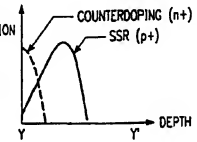


FIG. 4C

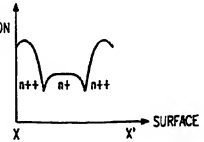


FIG. 4D

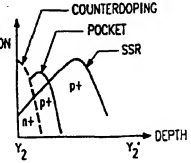


FIG. 5A

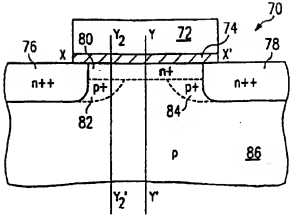


FIG. 5B

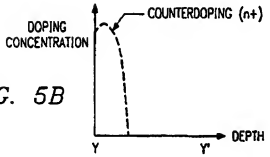


FIG. 5C

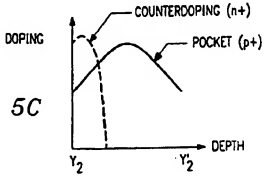


FIG. 5D

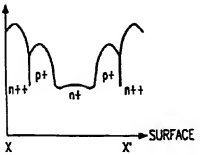


FIG. 6A

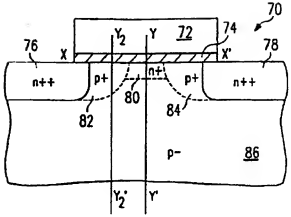


FIG. 6B

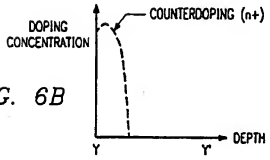


FIG. 6C

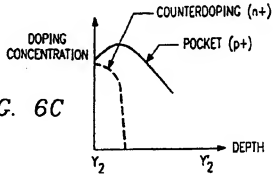


FIG. 6D